Exhibit A to Second Response to Office Action

CS152 Computer Architecture and Engineering

Lecture 5: Cost and Design

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lecture slides: http://www-inst.eecs.berkeley.edu/~cs152/

Die cost

Wafer cost

Dies per Wafer * Die yield

~ eff Wafer Area Dies per wafer

Die Area

Defects_per_unit_area

Die Yield =

Wafer yield

Die Cost is goes roughly with the cube of the area.

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Die Yield

		Raw Die	Raw Dices Per Wafer	Wafer		
wafer diameter	qi	die area (mm²)	mm^2			
	100	144	196	256	324	400
6"/15cm	139	06	62	4	32	23
8"/20cm	597	177	124	90	89	52
10"/25cm	431	290	206	153	116	06
die yield	23%	19%	16%	16% 12% 11%	11%	10%

typical CMOS process: ? =2, wafer yield=90%, defect density=2lcm2, 4 test sites/wafer

Testing!)	
(Before	
er Wafer	
d Dices F	
Good	

	7	5	6
)	က	7	13
•	S.	19 11	20
•	6	19	32
	16	32	53
	31	29	96
	6"/15cm	8"/20cm	10"/25cm

typical cost of an 8", 4 metal layers, 0.5um CMOS wafer: ~\$2000

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Real World Examples

Wafer Defect Area Dies/ Yield Die Cost cost Icm² wafer	360 71% \$4	54% \$			49		
Area L mm² w	43	8	121	196	234	256	200
Defect /cm²	1.0	1.0	1 .3	1.0	1.2	1.6	7
Wafer cost	\$900	\$1200	\$1700	\$1300	\$1500	\$1700	£1500
Line width	0.90	0.80		0.80	3 0.70	RC 3 0.70 \$1700	3 0.80 \$1500
Metal Line layers width		က	601 4	00 3		ARC 3	m
Chip	386DX	486DX2	PowerPC 601 4 0.80	HP PA 7100 3 0.80	DEC Alpha	SuperSPA	Pentium

From "Estimating IC Manufacturing Costs," by Linley Gwennap, Microprocessor Report, August 2, 1993, p. 15

Other Costs

Packaging cost Testing cost + Die cost IC cost =

Final test yield

Packaging Cost: depends on pins, heat dissipation

Chip	Die	a.	Package		Test &	Total	
	cost	pins	type		Assembly	1010	
386DX	\$4	132	QFP		44	9	
486DX2	\$12	168	PGA	\$11	\$ CF	9 9 C	
PowerPC 601	\$53	304	OFP	¥	7-0 4-0 7-0 8-0 8-0 8-0 8-0 8-0 8-0 8-0 8-0 8-0 8	1 0 1 0	
HP PA 7100	\$73	504		# C	- (7 7 6		
JEC Alpha	\$149	434	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	433	91¢	\$124	
SuperSPARC	\$272	293	PGA		\$23	\$202	
entium	\$417	273	PGA	\$19	404	\$320 \$473	

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